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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,155	10/27/2003	Ching-Nan Hsiao	10110752	3020
34283	7590	12/06/2004	EXAMINER	
QUINTERO LAW OFFICE 1617 BROADWAY, 3RD FLOOR SANTA MONICA, CA 90404			CHEN, JACK S J	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 12/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/694,155		HSIAO ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Jack Chen		2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### DETAILED ACTION

In response to the communication filed on September 9, 2004, claims 1-10 are active in this application.

#### *Terminal Disclaimer*

The terminal disclaimer filed on September 9, 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,670,246 has been reviewed and is accepted. The terminal disclaimer has been recorded.

#### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong, U.S./5,703,387.

Hong discloses a method for forming a semiconductor device, which comprises providing a substrate 32 having at least one trench 44 (figs. 3-5); forming doping areas as bit lines S/D (fig. 6) in the substrate near its surface and the bottom of the trench (fig. 6); forming bit line oxides 46 over each of the doping areas (fig. 7); forming a conformable insulating layer 50 (fig. 9) as gate

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dielectric *on the substrate surface that constitutes sidewalls* (NOTE: does not require direct contact) of the trench and the surface of the bit line oxide; and forming a conductive layer 52 (fig. 9) as a word line over the insulating layer and filling in the trench, see figs. 1-10; cols. 1-6 for more details.

Re claim 7, wherein the bit line oxides are formed by thermal oxidation (fig. 7; col. 3, line 62 to col. 4, line 7).

Re claim 8, wherein the bit line oxides have a thickness of about 600 angstroms (col. 4, lines 1-7).

Re claim 9, wherein the insulating layer is an ONO 50 (fig. 9; col. 4, lines 10-20).

Re claim 10, wherein the conductive layer is polysilicon (fig. 9; col. 4, lines 10-20).

3. Claims 1, 3-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hofmann et al., U.S./5,998,261.

Hofmann et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 1/3 having at least one trench (fig. 2); forming doping areas 14a/14b as bit lines in the substrate near its surface 14a/14b and the bottom 14a of the trench (fig. 3); forming bit line oxides 5/10 over each of the doping areas (figs. 3-4); forming a conformable insulating layer 12 (fig. 5) as gate dielectric *on the substrate surface that constitutes sidewalls* (NOTE: does not require direct contact) of the trench and the surface of the bit line oxide; and forming a conductive layer 13 (fig. 5) as a word line over the insulating layer and filling in the trench, see figs. 1-6; cols. 1-8 for more details.

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Re claim 3, wherein formation of the doped areas further comprises forming a spacer 8 over the sidewall of the trench; and performing ion implantation in the substrate using the spacer as a mask (fig. 3).

Re claim 4, wherein the spacer 8 is silicon nitride (fig. 3; col. 4, lines 9-15).

Re claim 5, inherently shows using phosphorus for ion implantation since phosphorus is n-type dopant (col. 4, lines 1-9).

Re claim 6, further removing the spacer before formation of the conformable insulating layer (figs. 3-5).

Re claim 7, wherein the bit line oxides are formed by thermal oxidation (fig. 4; col. 3, lines 38-45 and col. 6, lines 24-30).

Re claim 8, wherein the bit line oxides have a thickness of about 500 angstroms (col. 3, lines 38-45 and col. 6, lines 24-30).

Re claim 9, wherein the insulating layer 12 is an ONO (fig. 5; col. 4, lines 50-60).

Re claim 10, wherein the conductive layer 13 is polysilicon (fig. 5; col. 5, lines 1-10).

4. Claims 1, 7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al., U.S./6,486,028 B1.

Chang et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 100 having at least one trench (fig. 1); forming doping areas as bit lines 104/106/108 in the substrate near its surface and the bottom of the trench (fig. 2); forming bit line oxides 110 over each of the doping areas (fig. 3); forming a conformable insulating layer 112/114 (fig. 5) as gate dielectric *on the substrate surface that constitutes sidewalls* (NOTE: does not require direct contact) of the trench and the surface of the bit line oxide; and forming a

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conductive layer 116 (fig. 6) as a word line over the insulating layer and filling in the trench, see figs. 1-6; cols. 1-6 for more details.

Re claim 7, wherein the bit line oxides are formed by thermal oxidation (fig. 3; col. 3, lines 53-63).

Re claim 10, wherein the conductive layer is polysilicon (fig. 6; col. 4, lines 22-25).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, U.S./5,703,387.

Hong disclosed above; however, Hong is silent to forming the trench having a depth of about 1400 to 1600 angstroms.

But it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Hong by selecting the suitable depth for the trench, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann et al., U.S./5,998,261.

Hofmann et al. disclosed above; however, Hong is silent to forming the trench having a depth of about 1400 to 1600 angstroms.

But it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Hofmann et al. by selecting the suitable depth for the trench, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

### ***Response to Arguments***

9. Applicant's arguments filed September 9, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the gate dielectric directly contact the surface of the substrate) are not recited in the rejected claim(s).

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Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

### ***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen  
Primary Examiner  
Art Unit 2813

November 30, 2004